Analytical Approach to Optimize Routability in Consideration of Vias

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Motivation

Routing Resource Limits Block Area Scaling in Leading-edge Technologies

- The number of design rules has been ever increasing and getting more complicated as shown in Figure 1.
- In leading-edge technologies, scaling down of metal design rule is relatively behind of device, thus design implementation is likely to be troubled by routing resource
- Via is getting critical bottleneck in metal design rule, because via requires enough spacing to prevent process defects such as via not-open and via-to-via short
- Therefore, we will focus routing resource optimization in consideration of via in commercial 10nm technology
- We propose an idea : track re-alignment for signal routing

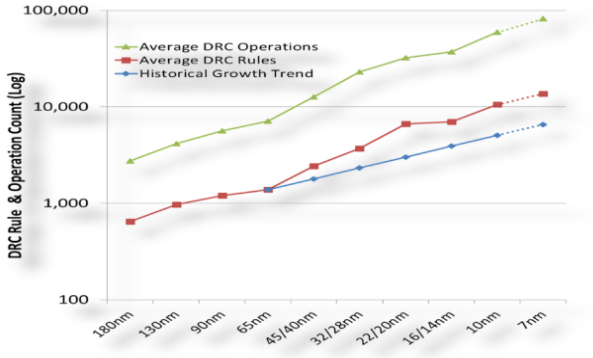


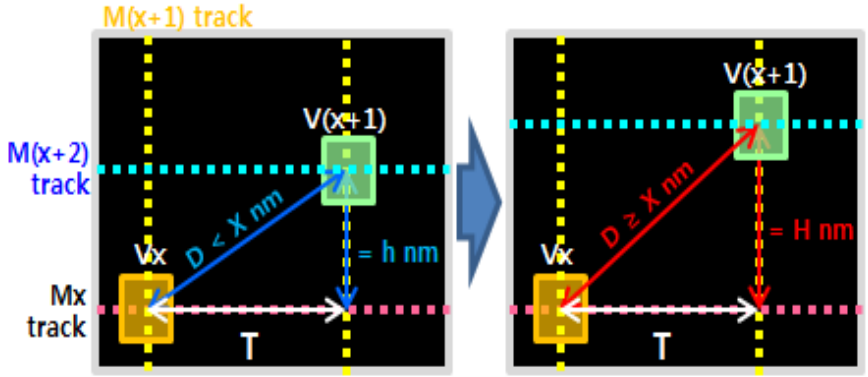
Figure 1. Increase in design rules in process nodes

[1] http://www.techdesignforums.com By John Ferguson

Track Re-alignment for Signal Routing

Concept

- Via is located on routing tracks as shown in Figure 2, and it must obey via-to-via spacing rule respect to different layers (e.g. Vx to Vx+1 layer spacing >= x nm)
- To put vias as close as possible for routing resource, h must be equals or larger than H $\geq\sqrt{(T^2+h^2)} \geq$ X, whereas "T" is Mx+1 layer metal pitch, it is known value
- We can control h by giving block-level offset btw Mx and Mx+2 routing layer such that frequency (# occurrence) of min h could be maximized in a block
- Heterogeneous metal stack is widely accepted in leading-edge technologies (4 1x metal layer, 3 1.7x metal layer, 2 2x metal layer), thus this process requires a mathematical way
- We model and solve a problem with ILP as shown in the following page



* X : Via spacing design rule between different via layers
* T : Track pitch for M(x+1)
* H : Distance which can satisfy the X rules
- H $\geq\sqrt{(T^2+h^2)}\geq$ X

Figure 2. Required distance to obey via spacing rule

Track Re-alignment for Signal Routing

ILP Modeling

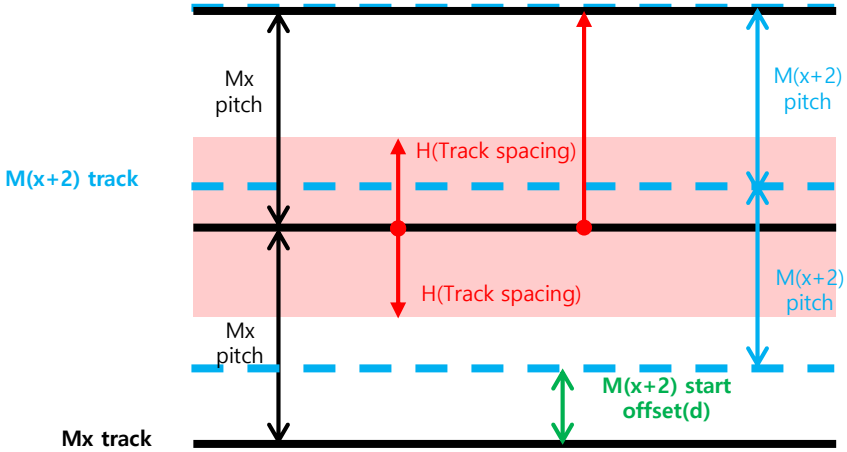


Figure 3. Example for ILP modeling

$$\sum_{k=1}^{K} x_{jk} = 1$$

$$x_{jk} = x_{(j+1)(k+M(x+2)pitch)} = \cdots = x_{(j+h)(k+M(x+2)pitch \times h)}$$

$$w_{ik} = \begin{cases} 1 \text{ if, } k \le M_{xi} - H \text{ or } k \ge M_{xi} + H \\ 0 \text{ otherwise} \end{cases}$$

Equation $T_i = \sum_{j=1}^{|J|} \sum_{k=1}^{K} w_{ik} \cdot x_{jk}$

$$T = \sum_{i=1}^{|I|} \sum_{j=1}^{|J|} \sum_{k=1}^{K} w_{ik} \cdot x_{jk}$$

$$\mathbf{d = k \text{ if, } } x_{0k} = 1 \textbf{ and maximum } T$$

1. Total # of Mx/M(x+2) track pairs (= T) should be maximum
   * Track pair : the pair of Mx & M(x+2) track which distance is more than offset
2. M(x+2) start offset(=d) < M(x+2) track pitch

Experimental Result

- **Case Study : 10nm Industrial test-cases implemented with commercial P&R tool**
  - Process node : 10nm
  - Target of via spacing rule
    : Via2 to Via3(center to center)
  - Consideration metal/via preferred direction track
    & metal pitch
    : Metal2(horizontal) / Metal4(horizontal)
    Metal3(vertical metal pitch)
  - Changed metal track's start offset : Metal4

Testcase		# of DRC	Total Logic Area	Signal Route Length	
				Target Metal (Metal4)	Total Metal Layers
Case1 (0.4M Instances)	Ref.	100%(*4885)	100%	100%	100%
	Ours	85.77%(*4190)	99.87%	99.60%	99.94%
	Imp.(%)	-14.23%	-0.13%	-0.40%	-0.06%
Case2 (3.6M Instances)	Ref.	100%(*2003)	100%	100%	100%
	Ours	55.42%(*1110)	99.14%	98.41%	98.61%
	Imp.(%)	-44.58%	-0.86%	-1.59%	-1.39%
Case3 (4.7M Instances)	Ref.	100%(416)	100%	100%	100%
	Ours	70.43%(293)	100.37%	96.37%	97.50%
	Imp.(%)	-29.57%	0.37%	-3.63%	-2.50%
	Avg.(%)	-29.46%	-0.21%	-1.88%	-1.32%

(*) : real number of DRC violations

Summary

- Via is getting important to utilization in leading-edge technologies, thus we proposed a way to optimize routability in consideration of design rule
- In signal routing, track re-alignment layer offset is proposed to maximize routing resource in consideration of vias in different layer
- We demonstrated that DRC violations(~45%) and total signal route length(~1.4%) can be reduced in 10nm industrial test cases.